High-Q LTCC-Based Passive Library for Wireless System-on-Package (SOP) Module Development

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***Abstract*—In this paper, we present the development and full characterization and modeling of a multilayer ceramic-based system-on-package component library. Compact high-Q three-dimensional inductor and capacitor topologies have been chosen and incorporated. A measured inductor Q factor as high as 100 and self-resonant frequency as high as 8 GHz have been demonstrated. The new vertically interdigitated capacitor topology occupies nearly an order of magnitude less of real estate while demonstrating comparable performance to the conventional topology. The low-temperature co-fired ceramic (LTCC) library has been incorporated into a 1.9-GHz CMOS power-amplifier design exhibiting a measured 17-dB gain, 26-dBm output power, and 48% power added efficiency. This power-amplifier module with fully integrated LTCC passives demonstrates a superior performance to those with full and partial on-chip passive integration.**

***Index Terms*—CMOS, high-Q inductors, LTCC, passive library, power amplifier.**

I. Introduction

THE system-on-package (SOP) concept [1] where components are integrated as part of the package housing the electronic system has been an attractive option to build wireless communications modules. Such a concept emerged out of the potential for a higher integration, which yields a more compact module size critical for portable applications. In addition, SOP components not only reduce the cost by eliminating the needs for discrete components and reducing the assembly time, but also have been demonstrated to exhibit superior performance to on-chip components [2], [3]. RF front-end building blocks such as the power amplifier often times require off-chip matching and biasing components [4], [5] since they can not be accommodated on-chip due to the Q and current-handling capability limitation. Multilayer low-temperature co-fired ceramic (LTCC) [6] is one of the popular SOP technologies. In addition to the capability of embedding components and interconnects, high-Q inductors have also been demonstrated [3].

In this paper, we report the first development of inductor and capacitor libraries incorporating compact architectures in a commercial 20-layer LTCC technology utilizing standard 3.6-mil-thick Dupont 951AT tapes [7]. The tapes have a dielectric constant of 7.8 and a loss tangent of 0.0015 at 10 MHz. Typical metallizations can be either 5-μm electroplated gold (surface and backside only), and 6-μm silver or silver–palladium alloy for surface, backside, or middle layers. Conventional design rules require a minimum of 4-mil linewidths and gaps, but recently allow as small as 1 mil utilizing the photo-imageable process. The multilevel ground plane and the vertically interdigitated capacitor (VIC) topologies chosen for the inductors and capacitors yield an inductor Q of as high as 100 with self-resonant frequency (SRF) as high as 8 GHz, while the VIC implementation demonstrates an area saving of nearly an order of magnitude compared to the conventional metal–insulator–metal (MIM) configuration. A 1.9-GHz CMOS power amplifier with fully integrated LTCC passives requiring no discrete components has been designed, fabricated, and measured for the first time at 1.9 GHz exhibiting 17-dB gain, 48% efficiency, and 26-dBm output power. This module demonstrates 7 dBm more output power, 7 dB more gain, and 28% more power-added efficiency (PAE) than the full-integrated-circuit (IC) implementation at the same frequency of 1.9 GHz.

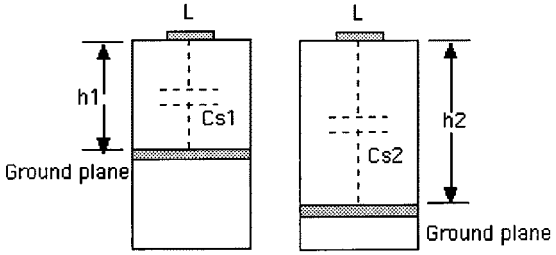

Fig. 1. Multilevel ground-plane inductor concept showing the cross section of two inductor structures having the same lateral dimension, but with different ground-plane locations in a multilayer board environment.

II. Inductor Library

The inductor library is built based on the multilevel ground plane concept illustrated in Fig. 1. In a multilevel ground-plane architecture, all the footprints of the components are on the surface layer, while the ground plane of each component may be on different levels. Such a topology has two advantages. First, by moving the location of the ground plane on different layers and maintaining the size of the inductor footprint, multiple inductance can be realized without occupying larger lateral real estate by increasing the number of turns. The effective inductance of the structure can be adjusted by increasing or reducing the shunt parasitic capacitor C_S in Fig. 1, causing reduction and

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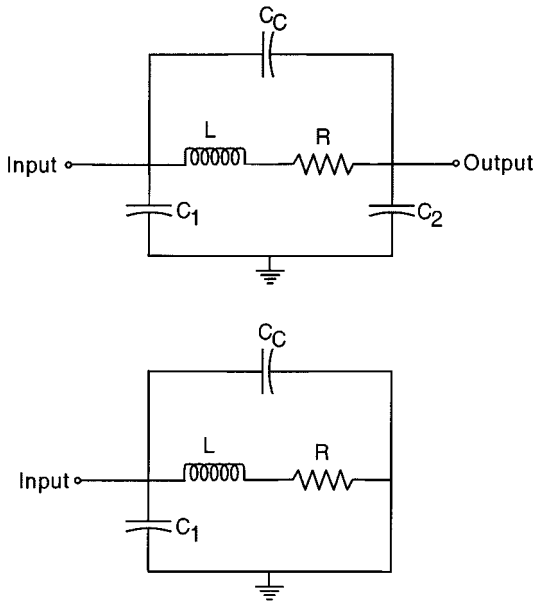


Fig. 2. One- and two-port electrical models for LTCC inductors.

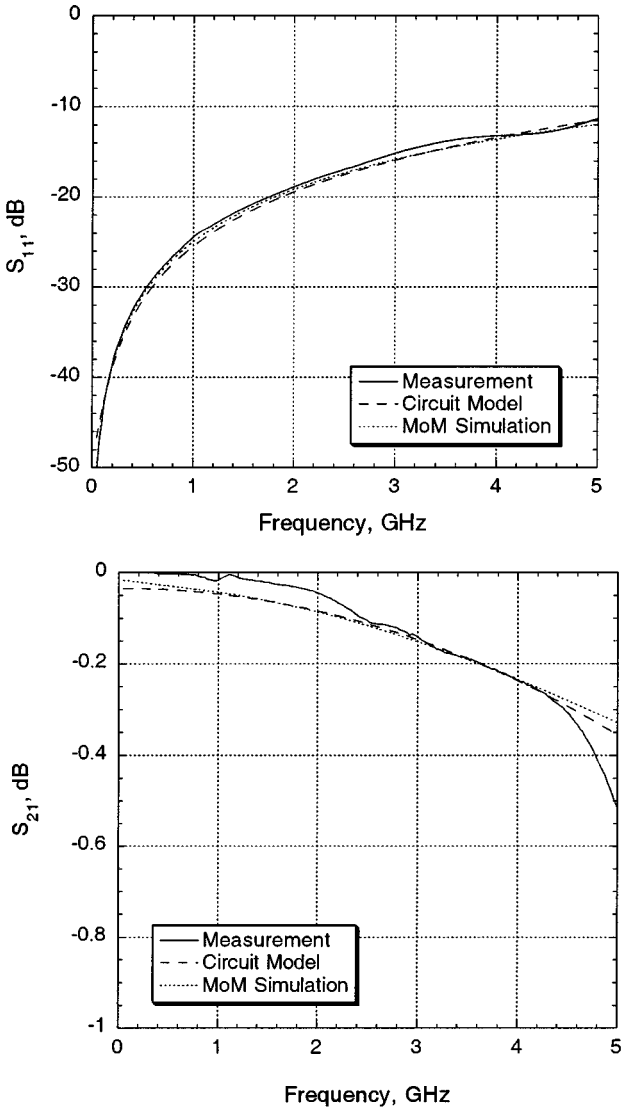


Fig. 3. Measured, electromagnetic, and circuit simulated magnitude plots of S-parameters for a 10-mil linewidth half-turn inductor with h of six layers (21.6 mil).

increase in effective inductance L_{eff}. Moving the ground plane closer to the inductor footprint increases C_S, thereby canceling part of the inductance. On the other hand, moving the ground plane further from the structure reduces C_S increases L_{eff}. In the example shown in Fig. 1, the inductor structure L in Fig. 1(a) has a closer gap to the ground plane than that in Fig. 1(b) ($h_1 < h_2$). Therefore, C_{s1} is larger than C_{s2}, implying $L_{\text{eff}1}$ is smaller than $L_{\text{eff}2}$. Close proximity of the ground plane to the inductor footprint reduces the effective inductance due to the negative mutual coupling caused by the current flowing in the ground plane in the opposite direction to the inductor current flow [8]. The reduction in L_{eff} consequently reduces Q and the SRF. However, we show experimentally that even though such phenomena occurs, a sufficiently high-Q and SRF can still be achieved. The second advantage of keeping the inductor footprint on the surface layer is to minimize the dielectric loss by maintaining part of the field of the inductor propagating in the air.

The inductor library consists of three different circular inductors, i.e., half, three-quarter, and full turns, with two different line widths, i.e., 10 and 20 mil, with ground planes ranging from 2 to 18 layers apart (h in Fig. 1). The upper half of the full-turn inductor was fabricated on the surface layer, while the other half was fabricated two layers below (7.2 mil apart). Some inductor test structures as part of the component library have been fabricated and measured to obtain their Q, L_{eff}, and SRF.

Standard high-frequency one- and two-port electrical model for inductors [9] were applied for LTCC inductors, as shown in Fig. 2. Shunt resistors to ground at the input and output ports typically incorporated in on-chip inductors to model the dielectric loss such as those on Si and GaAs are neglected in this case for two reasons. First, the loss tangent is sufficiently low and, secondly, the gap h, a minimum of 7.2 mil, is sufficiently large. The widely used inductor model often incorporates the coupling capacitor C_C in Fig. 2 to model the underpass capacitance at the output, as well as the inter-winding coupling. However, in this case, for example, for the half-turn inductors where there is no underpass and the inter-winding gap is sufficiently large, C_C can be neglected as well. In other configurations, C_C is also neglected to simplify the modeling process assuming C_C is "absorbed" by the shunt capacitors C_1 and C_2. Figs. 3–6 show the measured and modeled S-parameters of inductors fabricated using this concept. These structures were simulated using a commercial method-of-moments simulator [10]. In Figs. 3 and 4, the plots for a half-turn inductor with 10-mil linewidth and h equals six (21.6 mil) are shown. This inductor has the values of L, R, C_1, and C_2 of 1.2 nH, 0.35 Ω, 0.2 pF, and 0.2 pF, respectively. The inductor whose S-parameters are plotted in Figs. 5 and 6 is the same, except h is ten layers (36 mil). This configuration has L, R, C_1, and C_2 of 1.4 nH, 0.35 Ω, 0.15 pF, and 0.15 pF, respectively. The extracted model parameters demonstrate the usefulness of the multilevel ground-plane topology where using the same half-turn structure, and two different inductors with different inductance and shunt capacitances can be obtained.

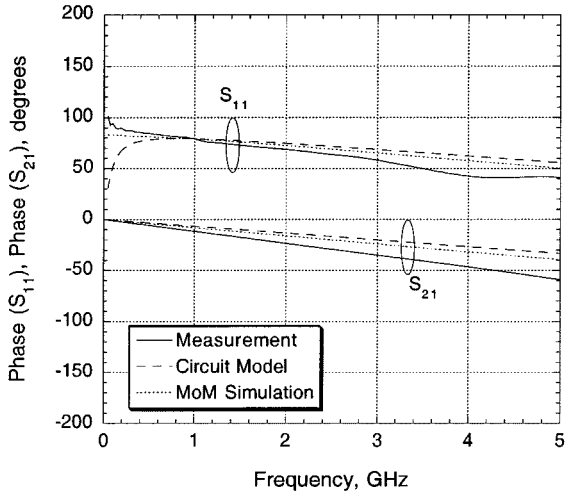


Fig. 4. Measured, electromagnetic, and circuit simulated phase plots of S-parameters for a 10-mil linewidth half-turn inductor with h of six layers (21.6 mil).

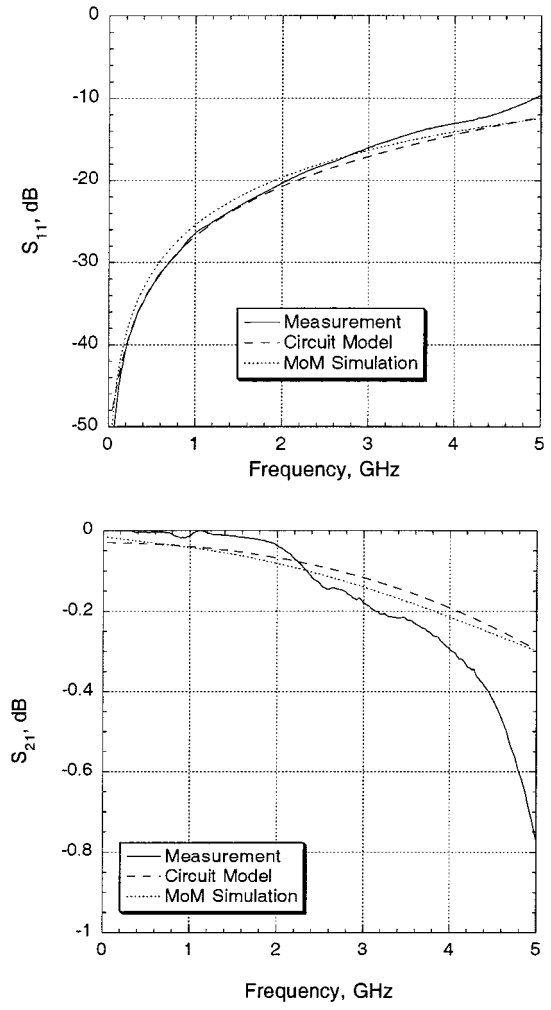


Fig. 5. Measured, electromagnetic, and circuit simulated magnitude plots of S-parameters for a 10-mil linewidth half-turn inductor with h of ten layers (36 mil).

One-port inductor test structures were fabricated as one-port microstrip devices in order to obtain their impedance and Q factor. The inductor Q was obtained by taking the ratio of the imaginary to the real part of the input impedance obtained from de-embedded S-parameters. The effective inductance L_{eff} is extracted experimentally by the ratio of the imaginary part of the impedance to the radial frequency ω. The Q, SRF, and L_{eff} of some inductor test structures are plotted in Figs. 7 and 8, indicating a high-Q performance in the frequency of interest at which the power amplifier was designed. As seen in Fig. 7, inductor Q as high as 100 at 2.9 GHz for a 1.4-nH inductor with the corresponding SRF of 8 GHz has been achieved. Table I summarizes the performance of the inductors plotted in Figs. 7 and 8. The multilevel ground-plane concept can be clearly seen by looking at different effective inductance L_{effs} achieved using the same inductor structures with the ground planes located at

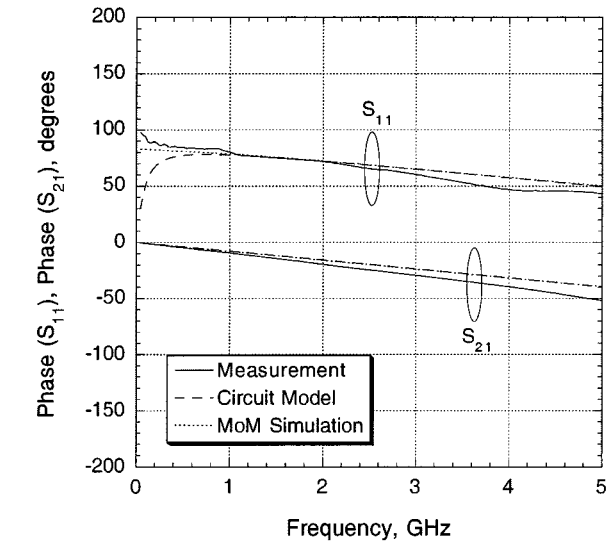


Fig. 6. Measured, electromagnetic, and circuit simulated phase plots of S-parameters for a 10-mil linewidth half-turn inductor with h of ten layers (36 mil).

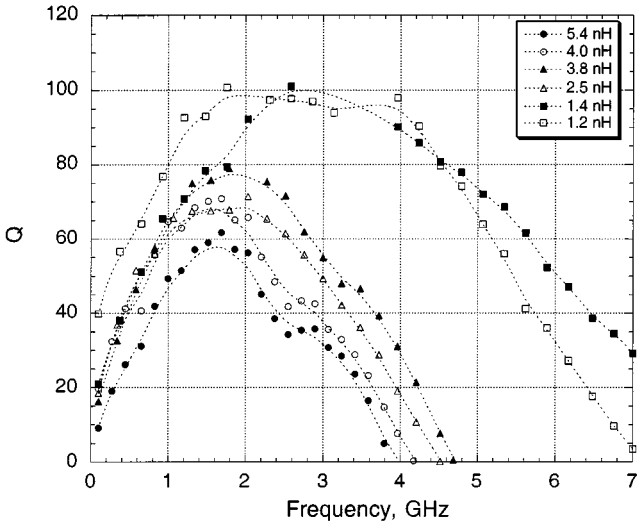


Fig. 7. Measured Q factor of one-port inductor test structures designed in a multilevel ground-plane topology.

TABLE I
SUMMARY OF MEASURED Q AND SRF OF INDUCTOR TEST STRUCTURES IMPLEMENTING THE MULTILAYER GROUND-PLANE CONCEPT

L_{eff} (nH)	Number of turns	Type	W (mils)	H (layers)	Q(1.9 GHz)	Qmax	SRF (GHz)
1.2	Three Quarter	Planar	20	2	100	100	7.2
1.4	Half	Planar	10	2	88	100	8
2.5	Three Quarter	Planar	10	2	70	70	4.5
3.8	Three Quarter	Planar	10	6	78	78	4.7
4	Full	3-D	10	2	65	70	4.2
5.4	Full	3-D	10	6	57	60	4

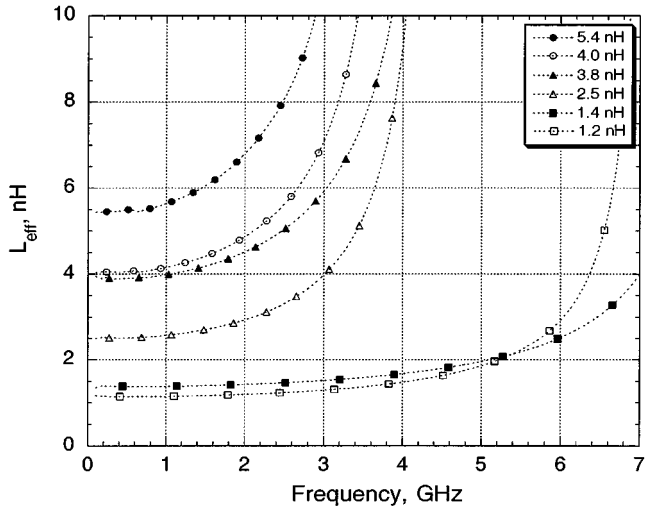


Fig. 8. Measured effective inductance ($L_{\rm eff}$) of one-port inductor test structures designed in a multilevel ground-plane topology.

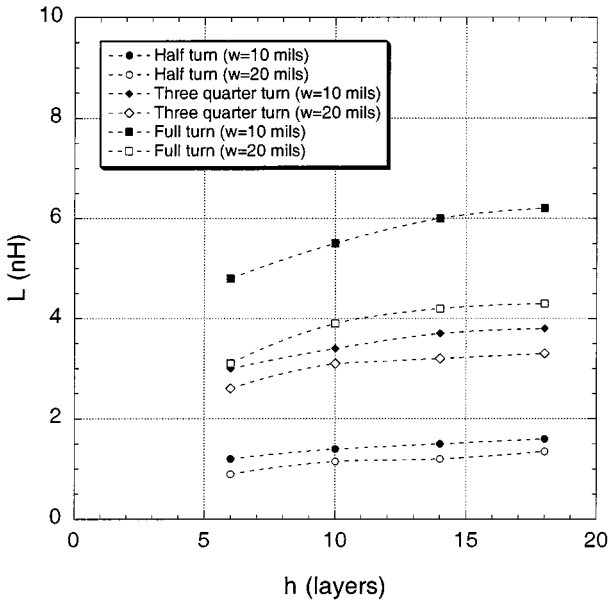


Fig. 9. Extracted inductance (L) as a function of the gap to the ground plane (h), number of turns, and linewidth.

different layers in Table I. For example, three-quarter-turn inductors with a distance to the ground plane h of two layers (7.2 mil) and six layers (21.6 mil) yield $L_{\rm effs}$ of 2.5 and 3.8 nH with the corresponding Q at 1.9 GHz of 70 and 78 and SRF of 4.5 GHz and 4.7 GHz, respectively. The inductor with h of six layers, in this case, exhibits about 200 MHz higher SRF due to less shunt capacitance to ground compared that with h of two layers. The Q of this inductor is also higher considering there is not as much as $L_{\rm eff}$ cancellation due to the negative mutual inductive coupling caused by the current flowing on the ground in the opposite direction to the current flow in the inductor [8], [11]. Also indicated in Table I, two full-turn inductors with h of two and six layers exhibit $L_{\rm eff}$ of 4 and 5.4 nH with the Q of 65 and 57 at 1.9 GHz and SRF of 4.2 and 4 GHz, respectively. The SRF of these two inductors seem to be counterintuitive since the one with h of six layers should have a higher SRF. However, note that the SRF not only depends on the parasitic capacitive mechanism, but also the $L_{\rm eff}$ of the structure [11].

A complete set of extracted model parameters based on the S-parameter measurements is shown in Figs. 9–11. These plots along with the series resistance R listed in Table II can be directly incorporated into the design process to establish a complete model for the LTCC inductors. Since the contribution of the eddy current flowing through the ground plane is negligible to the total loss compared to the conductor loss due to the inductor linewidth and length, the R is assumed to be independent of h. The plots in Figs. 9–11 can be interpolated to design inductors realized with h less than six layers. For example, a 2-nH inductor can be obtained using a three-quarter-turn inductor with 20-mil linewidth and h of four layers by interpolation from Fig. 9. The R for this inductor is 0.3 Ω according to Table II. Given h, the number of turns and linewidth, the interpolated input and output capacitances C_1 and C_2 from Figs. 10 and 11 are 0.46 and 0.48 pF, respectively.

It can be observed from Figs. 10 and 11 that C_1 and C_2 are nearly independent of h for h bigger than ten layers. It is also observed that for smaller h, the behavior of C_1 and C_2 are proportional to $1/h$, which follows the behavior of a parallel-plate capacitor. Therefore, since C_1 and C_2 are nearly independent of h for h greater than ten layers, the inductance L does not change

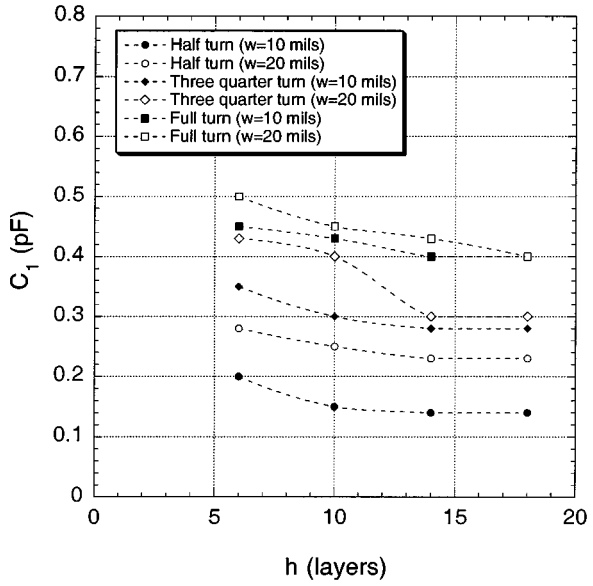


Fig. 10. Extracted input shunt capacitance (C_1) as a function of the gap to the ground plane (h), number of turns, and linewidth.

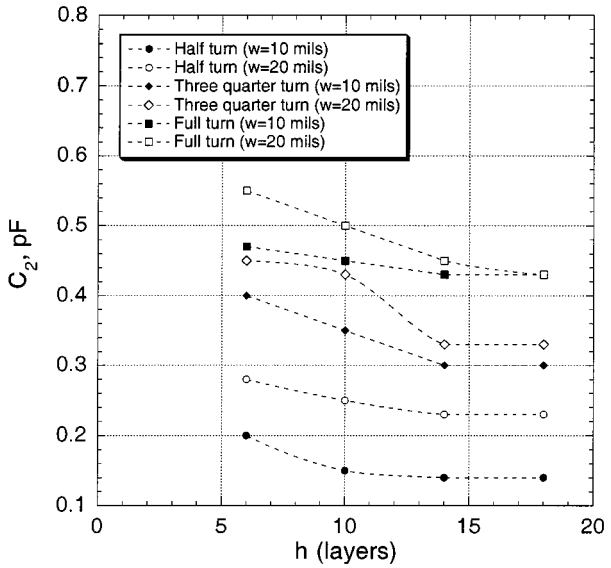
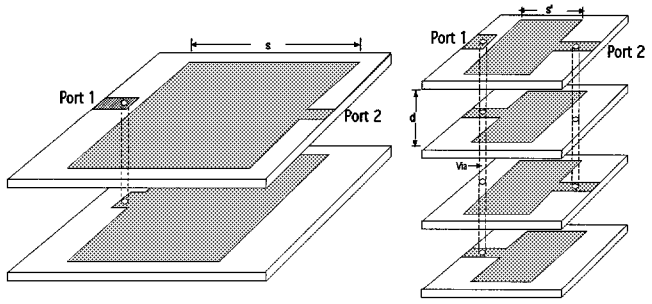


Fig. 11. Extracted output shunt capacitance (C_2) as a function of the gap to the ground plane (h), number of turns, and linewidth.

very much either, as confirmed by the plot in Fig. 9. Nevertheless, the change in L as small as 0.1 nH using the same lateral inductor structure is still often times useful to be incorporated in the design as well. The extracted series-resistance information can be obtained from Table II. For the inductors with the same number of turns and linewidths, the series-resistance R is assumed to be the same independent of h. Therefore, in the case of our 2-nH inductor made of a 20-mil three-quarter-turn inductor, the series resistance is 0.3 Ω. The model parameters supplied from this library and summarized in the plots in Figs. 9–11, as well as in Table II can be conveniently implemented as a database in a standard computer-aided design (CAD) tools similar to the implementation of passive database for semiconductor processes.

TABLE II
SUMMARY OF EXTRACTED SERIES RESISTANCE FOR THE HALF-, THREE QUARTER-, AND FULL-TURN LTCC INDUCTOR WITH 10- AND 20-mil LINEWIDTHS

# of turns	line width (mils)	R(Ω)
Half	10	0.35
Half	20	0.18
Three quarter	10	0.60
Three quarter	20	0.30
Full	10	0.70
Full	20	0.40



(a) (b)

Fig. 12. Three-dimensional views of a MIM and VIC configurations. (a) Parallel-plate capacitor. (b) VIC.

III. CAPACITOR LIBRARY

Conventional MIM capacitors [12] in microstrip configuration are incorporated for the capacitor library. A capacitance of 0.48 fF/mil^2 can be achieved using standard 3.6-mil-thick tapes. A 4.9-pF MIM, for example, can be realized by a 100 mil $\times$ 100 mil square electrodes neglecting the fringing fields. The ground planes for two-port MIMs are chosen to be as far as possible from the MIM electrodes to minimize parasitics. The one-port MIMs are formed by one electrode on the surface layer and the layer below it which also serves as the ground plane. The size of MIM capacitors are acceptable for small capacitors such as those used in the transformation network for design frequency ranging from around 900 MHz and above. For large capacitors such as the RF ground capacitors, however, the electrode size becomes impractical. Therefore, there is a need for a new configuration to maintain the compactness of the capacitor structures. The lateral electrode interdigitation method [13] has been applied to implement a capacitor as well. While exhibiting less parasitics, this topology tends to require a bigger area considering the electric flux is generated laterally instead of vertically, such as in the MIM case, which allows more electrode coverage and, thus, occupies less area.

An alternative capacitor implementation to the MIM topology was proposed using the VIC. Fig. 12(b) illustrates the concept of the VIC as compared to the conventional MIM structure shown in Fig. 12(a). The MIM structure consisting of a dielectric layer sandwiched between two square plates of width s in Fig. 12(a) implements a capacitor with the capacitance given by $C = \varepsilon_0 \varepsilon_r s^2/d$ neglecting the higher order excitation mode. This capacitor can also be implemented by a parallel combination of pairs of plates of smaller size. The VIC deploys these smaller

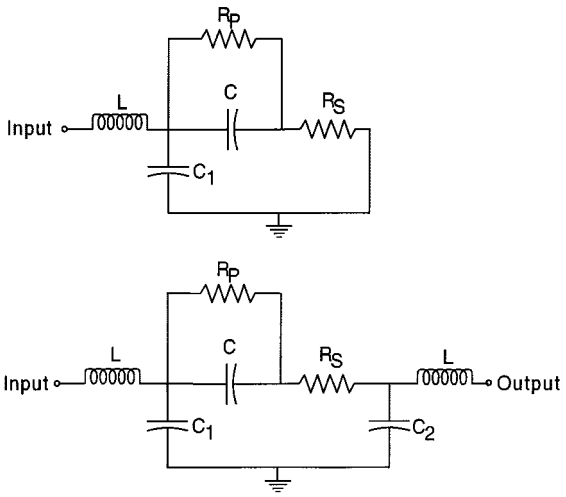


Fig. 13. One- and two-port electrical models for LTCC capacitors.

plates with width s' vertically, as depicted in Fig. 12(b). The plate size can be made smaller as more plates are deployed on more dielectric layers. The electric flux not only flows vertically between the pair of the capacitor electrodes, but also laterally between the via interconnects to the electrode. Such a mechanism allows further shrinkage of the VIC plates. The VIC is a suitable architecture to realize an extremely compact capacitor. The one- and two-port lumped-element models for the LTCC capacitors is drawn in Fig. 13 consisting of a series capacitor C in series with a series resistor R_S to model the conductor loss and a resistor R_P in parallel with C to model the dielectric loss. The capacitors C_1, C_2, and the inductor L in the schematics shown in Fig. 13 represent the shunt parasitic capacitance and inductance, respectively. The MIM capacitors in the library were designed using the well-known formula for parallel-plate capacitors. Assuming the shape of the MIM electrode is square with side width s to implement a capacitor C given by $C = \varepsilon_0 \varepsilon_r s^2/d$ where d is the tape thickness utilizing the standard 3.6-mil tapes, the actual drawn side width is about 0.9 s to account for the fringing effects.

For testing purposes, we fabricated a 1.4- and 6.2-pF capacitors in both VIC and MIM configurations by incorporating the effects of the fringing fields. The plate size for the 1.4- and 6.2-pF MIM capacitors are 45 mil $\times$ 45 mil and 101 mil $\times$ 101 mil, respectively. Both VICs were fabricated using plates including the ground plane on five tape layers similar to those illustrated in Fig. 13(b). The size of each plate for the 1.4- and 6.2-pF VICs is 18 mil $\times$ 18 mil and 47 mil $\times$ 47 mil, respectively. The VIC implementation saves over 75% of the real estate compared to the MIM implementation. A one-port capacitor can be realized by simply connecting the bottom electrode of the MIM structure to ground or using the ground itself as the bottom electrode. For the VIC, the electrodes connected to one of the ports in Fig. 13(b) were simply shorted to ground to realize a one-port device.

Fig. 14 shows the measured effective capacitance C_{eff} and Q as a function of frequency superimposed with the MoM [10] and circuit simulation for the 1.4-pF capacitors implemented in the MIM and VIC configurations. The measured nominal values of

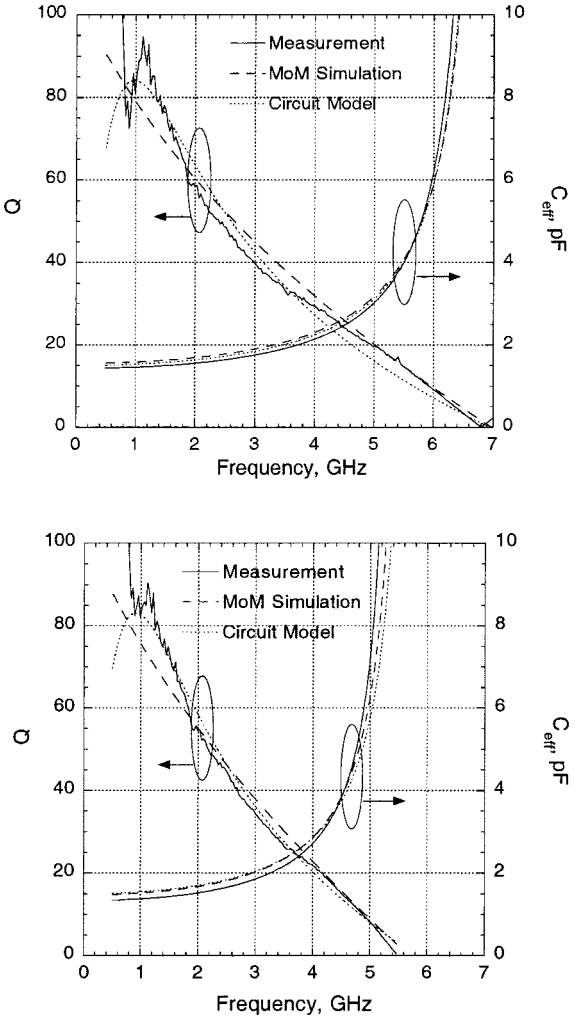


Fig. 14. Measured, electromagnetic, and circuit simulated Q and effective capacitance (C_{eff}) for a 1.4-pF capacitors designed in MIM (top) and VIC configurations (bottom).

C_{eff} for both capacitor topologies are 1.4 pF. The VIC capacitor exhibits a slightly less Q and SRF than the MIM implementations. The vias connecting the VIC plates present an additional parasitic inductance, which lowers the SRF. In addition to the inductive effects, more conductor loss caused by the vias contributes to the total loss mechanism of the VIC structures, which consequently affects the Q factor as well. This is demonstrated by the extracted model parameters using the schematic in Fig. 13 for the 1.4-pF MIM with C, C_1, L, R_S, R_P of 1.4 pF, 0.1 pF, 0.35 nH, 0.7 Ω, and 18 kΩ, respectively. The extracted model parameters for the 1.4-pF VIC capacitor is 1.4 pF, 0.1 pF, 0.5 nH, 0.75 Ω, and 19 kΩ, respectively, for C, C_1, L, R_S, and R_P, respectively. It is demonstrated here that the VIC exhibits 0.05 Ω more series resistance and 0.15 nH more parasitic inductance due to the vias interconnecting the VIC electrodes. The measured effective capacitance C_{eff} and Q as a function of frequency superimposed with the MoM [10] and circuit simulation for the 6.2-pF capacitors implemented in the MIM and VIC configurations are plotted in Fig. 15. The extracted model parameters for the 6.2-pF MIM are 6.2 pF, 0.1 pF, and 0.4 nH and 0.2 Ω and 18 kΩ for C, C_1, L, R_S, and R_P, respectively, while

TABLE III
MEASURED PERFORMANCE COMPARISON OF TWO CAPACITORS 1.4 AND 6.2 pF; EACH IMPLEMENTED IN MIM AND VIC CONFIGURATIONS

No.	Type	Plate size (mil x mil)	Lateral Capacitor Area (mil^2)	Number of plates	Nominal C_{eff} (pF)	SRF (GHz)
1	MIM	45	2025	2	1.4	6.8
2	VIC	18	324	5	1.4	5.5
3	MIM	101	10,201	2	6.2	3.1
4	VIC	47	2,209	5	6.2	2.4

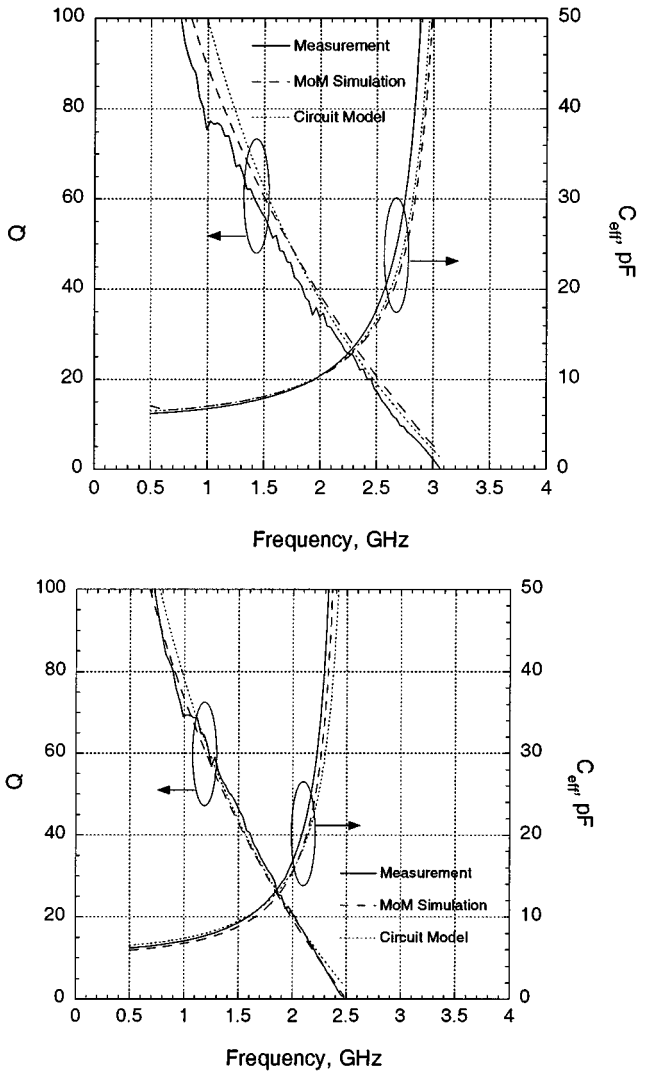


Fig. 15. Measured, electromagnetic, and circuit simulated Q and effective capacitance ($C_{\rm eff}$) for a 6.2-pF capacitors designed in MIM (top) and VIC configurations (bottom).

for the corresponding VIC implementation, the parameters are 6.2 pF, 0.1 pF, and 0.6 nH and 0.25 Ω and 19 kΩ, respectively. In this case, the VIC exhibits 0.05 Ω more series resistance and 0.2 nH more parasitic inductance as confirmed by the measured results in Fig. 15. Table III outlines the measured performance comparisons of the two capacitors fabricated in MIM and VIC configurations.

IV. 1.9-GHz CMOS-LTCC POWER AMPLIFIER

As a demonstration vehicle, a two-stage class-F power amplifier for a digital enhanced cordless telephone (DECT) using

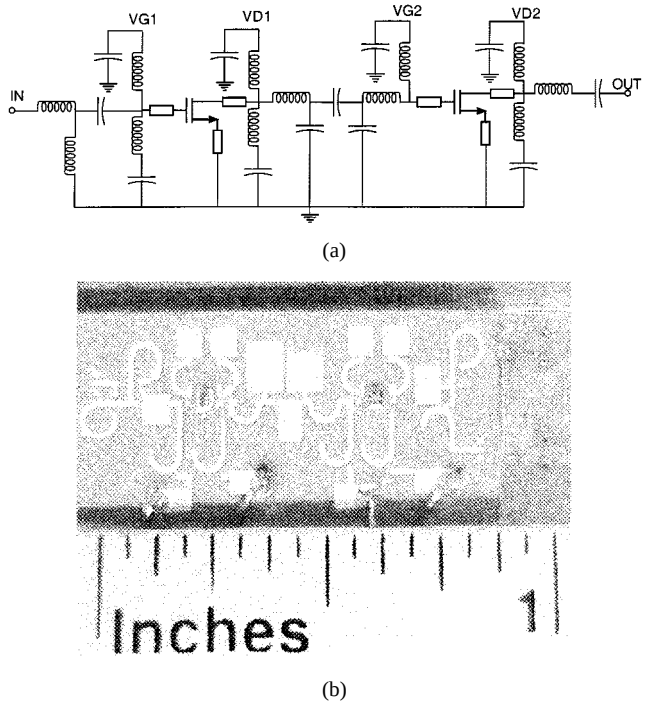


Fig. 16. (a) Schematic diagram of the 1.9-GHz CMOS-LTCC power amplifier. (b) LTCC power-amplifier module with NMOS devices wire bonded on the board.

Si-NMOS active devices has been built utilizing components from the library. Fig. 16(a) and (b) shows the circuit schematic and photograph of the LTCC circuit occupying a 0.9 in × 0.5 in board area. The two NMOS devices fabricated in a standard 0.8-μm CMOS technology were wire bonded onto gold pads on the LTCC board.

A custom RF/microwave nonlinear MOSFET model for large-signal applications was used for this design and demonstrates compatibility with standard commercial wireless CAD tools [14]. The half-turn and three-quarter-turn inductors were used as matching components, while the full-turn inductors were used as RF chokes. Parallel-plate MIM capacitors were utilized as matching components since their values and sizes are relatively small. The RF ground capacitors were implemented in VIC topologies since they require large capacitance and area. Second harmonic tuning elements were implemented by a series *LC* resonators at 3.8 GHz. The area saving of the VIC can be clearly observed in Fig. 16(b). The electrodes where the dc-bias cables are soldered are the top electrodes of the RF ground VICs. The size advantage of the VIC is obvious by comparing the size of those electrodes to other MIM capacitor electrodes used in the matching network and harmonic tuning some of which occupy an even larger area than the RF ground VICs.

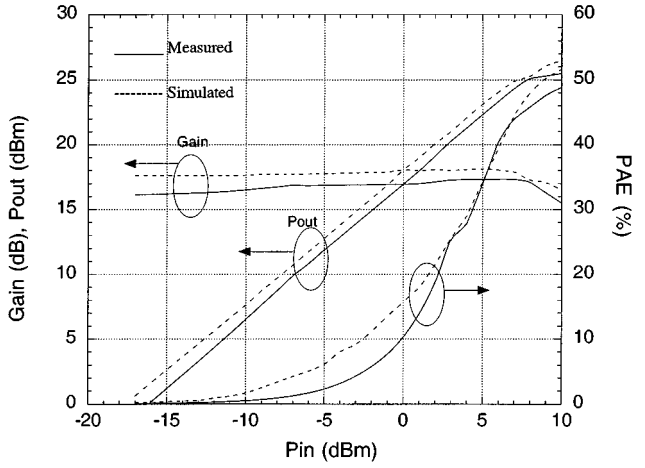


Fig. 17. Measured and simulated output power, gain, and efficiency at 1.9 GHz of the CMOS power-amplifier module with fully integrated LTCC passives.

TABLE IV
SUMMARY OF MEASURED AND SIMULATED PERFORMANCE OF THE 1.9-GHz CMOS POWER–AMPLIFIER MODULE WITH FULLY INTEGRATED LTCC PASSIVES

Specification	Simulation Data	Measured Data
Freqency Range	1.88 GHz to 1.9 GHz	1.88 GHz to 1.9 GHz
Supply Voltage	3.3 V	3.3 V
Maximum Pout	27 dBm	26 dBm
Input VSWR	<1.5:1	<1.5:1
Gain Variation In Band	<0.5 dB	<0.8 dB
Power Added Efficiency	51 %	48 %
Power Gain	18 dB	17 dB

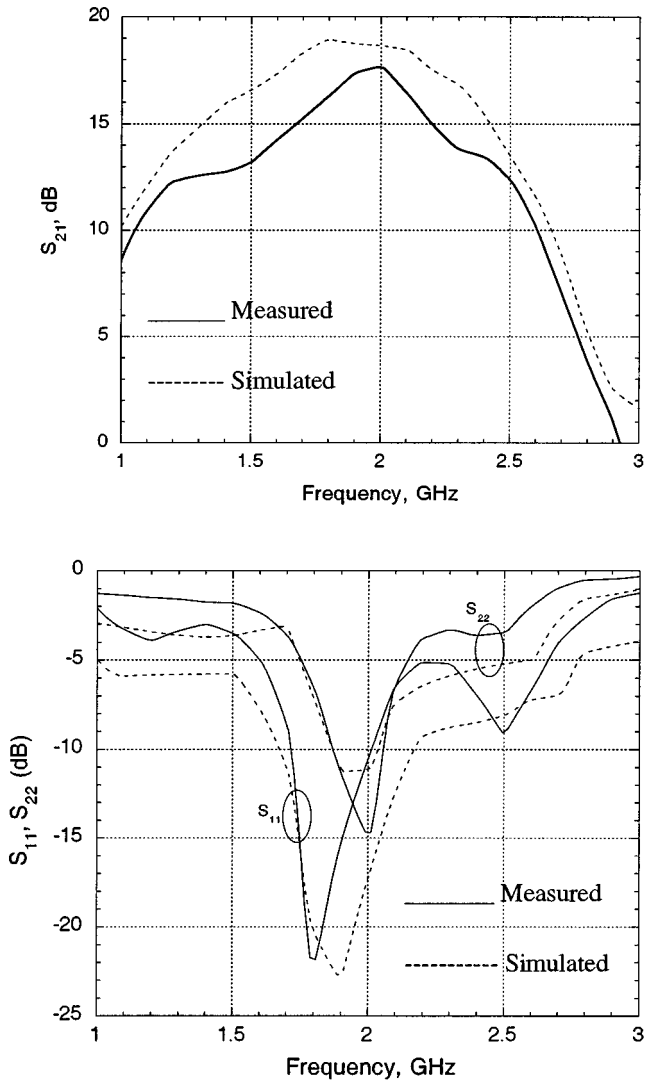


Fig. 18. Measured and simulated small-signal S-parameter of the CMOS power amplifier module with fully integrated LTCC passives.

While this circuit represents the first application of the component library where all passives are integrated based on the library, it may not be the most area-efficient option for a compact module. Alternative solutions include integrating "noncritical" passives such as the RF choke inductors and RF ground capacitors on-chip and integrate the rest of the passives on the LTCC and/or integrating the interstage matching network on-chip.

The measured and simulated gain, output power, and PAE at 1.9 GHz are plotted in Fig. 17. The power amplifier exhibits a measured 17 dB of gain, 26 dBm of output power, and 48% PAE at 3.3-V supply voltage. These results represent an improved performance compared to earlier data presented in [7] with 3-V power supply. Fig. 18 plots the measured and simulated small-signal performance of the power amplifier, indicating a measured 17 dB of gain and better than 15-dB input and output return losses in the 1.88–1.9-GHz range. A detailed summary of the circuit performance is outlined in Table IV. A slight discrepancy observed in Figs. 17 and 18, as well as in Table IV, between the simulated and measured data is attributed to the discontinuous ground plane of the circuit inherent to the LTCC circuit topologies incorporating the multilevel ground-plane library. An additional loss mechanism caused by the vias connecting the ground planes of the circuit located on different layers contributes to a difference in the measured performance. This mechanism was not accounted for during the simulation and requires a separate characterization to quantify its effect on the circuit performance. Nonetheless, the simulated results are able to predict reasonably well the actual circuit performance.

To investigate the advantage of integrating passives on-package such as on the LTCC, another 1.9-GHz power amplifier was built with the same topology as that with fully integrated LTCC passives. The two-stage CMOS power amplifier integrated the interstage matching components on-chip, while the input and output matching elements, as well as the RF choke and ground inductors and capacitors, were integrated on the LTCC using the library components. Half-, quarter-, and full-turn inductors, as well as square and rectangular parallel-plate capacitors from the LTCC library, were utilized in this circuit. The VICs could have also been incorporated in this design. However, since a smaller area was anticipated, a parallel —plate capacitor configuration was chosen to obtain a better performance. Fig. 19 shows the circuit schematic and the photograph of the LTCC board housing the module occupying a 511 mil $\times$ 472 mil area, nearly one-half the size of the module with fully integrated LTCC passives. The simulated

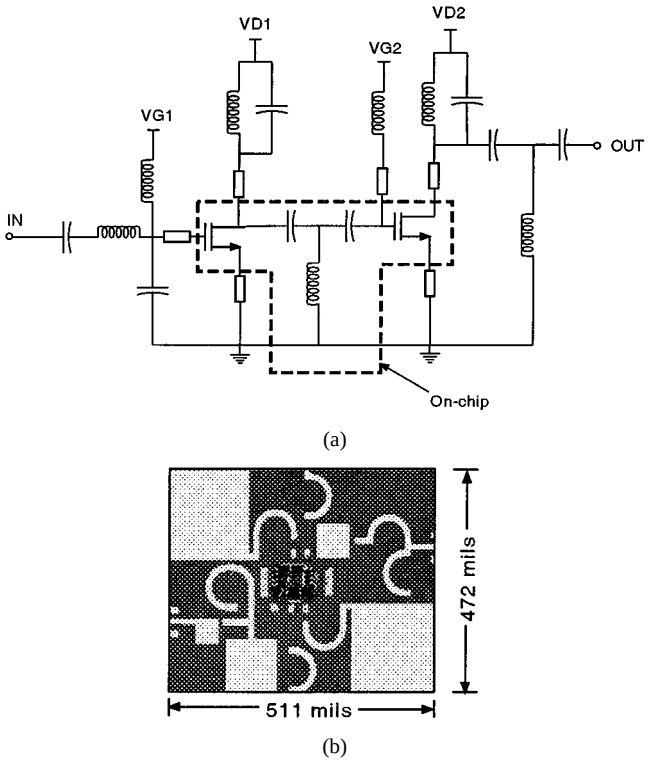


Fig. 19. (a) Circuit schematic and (b) photograph of the 1.9-GHz CMOS power amplifier with on-chip interstage matching and LTCC integrated input/output matching.

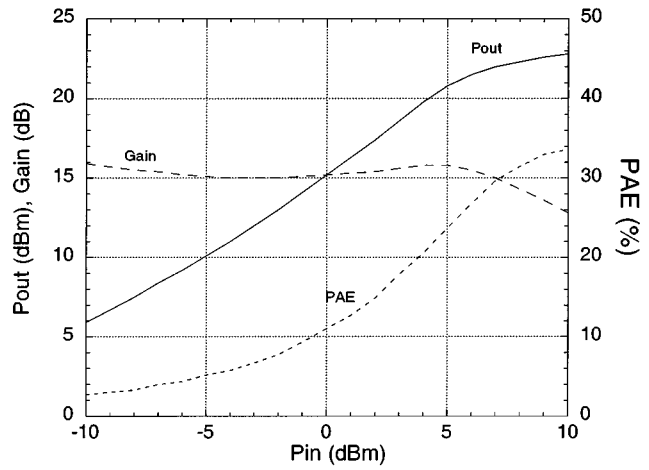


Fig. 20. Measured output power, PAE, and gain at 1.9 GHz of the CMOS power amplifier with on-chip interstage matching and LTCC-integrated input/output matching.

results of this circuit are not as accurate as those demonstrated by the fully on-package PA module due to the difficulty and complexity of modeling CMOS inductors and capacitors.

Fig. 20 shows the plots of the measured output power, PAE, and gain of this circuit. A measured 23 dBm of output power, 32% PAE, and 15 dB of gain were achieved using this hybrid-passive integration approach. Implementing interstage matching elements on-chip causes 3 dBm less output power, 16% less PAE, and 2 dB less gain with the advantage of occupying smaller real estate when compared to the fully on-package passive integration whose performance is summarized in Table IV.

TABLE V
MEASURED PERFORMANCE SUMMARY OF THREE DIFFERENT 1.9-GHz CMOS POWER AMPLIFIERS WITH THREE DIFFERENT TYPES OF PASSIVE COMPONENT INTEGRATION

Passive Integration	Pout (dBm)	Gain (dB)	PAE (%)	Area (mil x mil)
Fully-on-package	26	17	48	900 x 500
On-chip interstage	23	15	32	511 x 472
Fully on-chip	19	10	20	105 x 84

The fully monolithic, i.e., the fully on-chip version of this power amplifier using the same CMOS technology and the same schematic as that shown in Fig. 19, has also been designed, fabricated, and measured [15]. This power-amplifier IC occupying a silicon area of 105 mil $\times$ 84 mil exhibits a measured output power, PAE, and gain of 19 dBm, 20%, and 10 dB, respectively. When compared to the fully on-package passive integrated circuit, the power-amplifier IC shows 7 dBm less output power, 28% less PAE, and 7 dB less gain while occupying nearly an order of magnitude less area. Compared to the partial on-chip approach, the fully monolithic circuit demonstrates 4 dBm less output power, 12% less efficiency, and 5 dB less gain. These results clearly demonstrate the advantages of implementing on-package components where superior Q performance can be achieved. Table V outlines the measured performance comparison of the 1.9-GHz power amplifier employing three different passive integration approaches, fully LTCC integrated, on-chip interstage integrated, and fully on-chip integrated techniques.

V. CONCLUSION

In this paper, we have reported for the first time the development of an LTCC-based component library for wireless RF SOP applications. The library incorporates compact inductor and capacitor topologies demonstrating a Q performance as high as 100 and the corresponding SRF of 8 GHz for a 1.4-nH inductor overcoming the Q-limitation typically encountered for on-chip passives. The library components have been incorporated into a fully functional 1.9-GHz CMOS DECT power amplifier with fully integrated LTCC passives exhibiting 17 dB of gain, 26-dBm output power, and 48% PAE. This module exhibits 7 dBm more output power, 7 dB additional gain, and 28% more PAE than the fully monolithic PA at 1.9 GHz.

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